FUJITSU SEMICONDUCTOR
DATA SHEET

DS05-11245-1E

MEMORY

Unbuffered

4 M × 64 BIT HYPER PAGE MODE DRAM DIMM

MB8504E064AB-60/-70

Unbuffered, 4 M × 64 Bit Hyper Page Mode DIMM, 3.3 V, 1-bank, 2 KR

■ DESCRIPTION

The Fujitsu MB8504E064AB is a fully decoded, CMOS Dynamic Random Access Memory (DRAM) module consisting of sixteen MB81V17405A devices. The MB8504E064AB is optimized for those applications requiring small size package, low power consumption, enhanced performance. The operation and electrical characteristics of the MB8504E064AB are the same as the MB81V17405A which features hyper page mode (EDO) operation. For ease of memory expansion, the MB8504E064AB is offered in an 168-pin Dual In-line Memory Module package (DIMM).

■ PRODUCT LINE & FEATURES

Parameter		MB8504E064AB	
		-60	-70
$\overline{RAS}$ Access Time		60 ns max.	70 ns max.
Random Cycle Time		104 ns min.	124 ns min.
Address Access Time		30 ns max.	35 ns max.
$\overline{CAS}$ Access Time		15 ns max.	17 ns max.
Hyper Page Mode Cycle Time		25 ns min.	30 ns min.
Power Dissipation	Operating Mode	6336 mW	5472 mW
	Standby Mode	115.2 mW	115.2 mW

- Conformed to 168-pin Unbuffered DIMM JEDEC standard
- Organization : 4,194,304 words × 64 bits
- Module Size : 1.0” (height) × 2.66” (length) × 0.35” (thickness)
- Memory : MB81V17405A (4 M × 4, 2 K ref., 3.3 V) 16 pcs
- 3.3 V ± 0.3 V Supply Voltage
- 2,048 Refresh Cycles / 32.8 ms
- Hyper Page Operation (EDO)
- Serial Presence Detect
- JEDEC standard Serial PD Format
- $\overline{RAS}$-Only Refresh / $\overline{CAS}$-before-$\overline{RAS}$ Refresh

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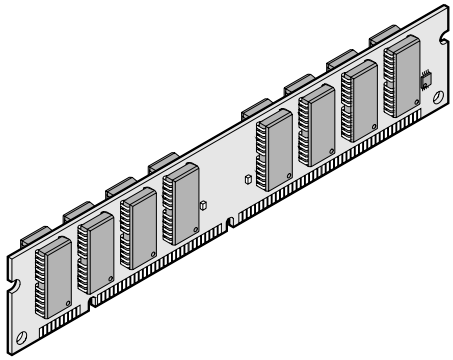
■ PACKAGE

168-pin plastic DIMM



(MDS-168P-P11)

Package and Ordering Information

– 168-pin DIMM, order as MB8504E064AB-××DG (DG = Gold Pad)

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■ PIN ASSIGNMENTS

Pin No.	MB8504E064AB	Pin No.	MB8504E064AB	Pin No.	MB8504E064AB	Pin No.	MB8504E064AB
1	V_{SS}	43	V_{SS}	85	V_{SS}	127	V_{SS}
2	DQ_0	44	$\overline{OE}_2$	86	DQ_{32}	128	N.C.
3	DQ_1	45	$\overline{RAS}_2$	87	DQ_{33}	129	N.C.
4	DQ_2	46	$\overline{CAS}_2$	88	DQ_{34}	130	$\overline{CAS}_6$
5	DQ_3	47	$\overline{CAS}_3$	89	DQ_{35}	131	$\overline{CAS}_7$
6	V_{CC}	48	$\overline{WE}_2$	90	V_{CC}	132	N.C.
7	DQ_4	49	V_{CC}	91	DQ_{36}	133	V_{CC}
8	DQ_5	50	N.C.	92	DQ_{37}	134	N.C.
9	DQ_6	51	N.C.	93	DQ_{38}	135	N.C.
10	DQ_7	52	N.C.	94	DQ_{39}	136	N.C.
11	DQ_8	53	N.C.	95	DQ_{40}	137	N.C.
12	V_{SS}	54	V_{SS}	96	V_{SS}	138	V_{SS}
13	DQ_9	55	DQ_{16}	97	DQ_{41}	139	DQ_{48}
14	DQ_{10}	56	DQ_{17}	98	DQ_{42}	140	DQ_{49}
15	DQ_{11}	57	DQ_{18}	99	DQ_{43}	141	DQ_{50}
16	DQ_{12}	58	DQ_{19}	100	DQ_{44}	142	DQ_{51}
17	DQ_{13}	59	V_{CC}	101	DQ_{45}	143	V_{CC}
18	V_{CC}	60	DQ_{20}	102	V_{CC}	144	DQ_{52}
19	DQ_{14}	61	N.C.	103	DQ_{46}	145	N.C.
20	DQ_{15}	62	N.C.	104	DQ_{47}	146	N.C.
21	N.C.	63	N.C.	105	N.C.	147	N.C.
22	N.C.	64	V_{SS}	106	N.C.	148	V_{SS}
23	V_{SS}	65	DQ_{21}	107	V_{SS}	149	DQ_{53}
24	N.C.	66	DQ_{22}	108	N.C.	150	DQ_{54}
25	N.C.	67	DQ_{23}	109	N.C.	151	DQ_{55}
26	V_{CC}	68	V_{SS}	110	V_{CC}	152	V_{SS}
27	$\overline{WE}_0$	69	DQ_{24}	111	N.C.	153	DQ_{56}
28	$\overline{CAS}_0$	70	DQ_{25}	112	$\overline{CAS}_4$	154	DQ_{57}
29	$\overline{CAS}_1$	71	DQ_{26}	113	$\overline{CAS}_5$	155	DQ_{58}
30	$\overline{RAS}_0$	72	DQ_{27}	114	N.C.	156	DQ_{59}
31	$\overline{OE}_0$	73	V_{CC}	115	N.C.	157	V_{CC}
32	V_{SS}	74	DQ_{28}	116	V_{SS}	158	DQ_{60}
33	A_0	75	DQ_{29}	117	A_1	159	DQ_{61}
34	A_2	76	DQ_{30}	118	A_3	160	DQ_{62}
35	A_4	77	DQ_{31}	119	A_5	161	DQ_{63}
36	A_6	78	V_{SS}	120	A_7	162	V_{SS}
37	A_8	79	N.C.	121	A_9	163	N.C.
38	A_{10}	80	N.C.	122	N.C.	164	N.C.
39	N.C.	81	N.C.	123	N.C.	165	SA_0
40	V_{CC}	82	SDA	124	V_{CC}	166	SA_1
41	V_{CC}	83	SCL	125	N.C.	167	SA_2
42	N.C.	84	V_{CC}	126	N.C.	168	V_{CC}

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■ PIN DESCRIPTIONS

Symbol	Function	Input/Output	Pin Count
A_0 to A_{10}	Address Input	Input	11
$\overline{RAS}_0$ and $\overline{RAS}_2$	Row Address Strobe	Input	2
$\overline{CAS}_0$ to $\overline{CAS}_7$	Column Address Strobe	Input	8
$\overline{WE}_0$ and $\overline{WE}_2$	Write Enable	Input	2
$\overline{OE}_0$ and $\overline{OE}_2$	Output Enable	Input	2
DQ_0 to DQ_{63}	Data-input/Data-output	Input/Output	64
SCL	Serial PD Clock	Iutput	1
SDA	Serial PD I/O	Input/Output	1
SA_0 to SA_2	Serial PD Address Input	Input	3
V_{CC}	Power Supply	—	17
V_{SS}	Ground	—	18
N.C.	No Connection	—	39

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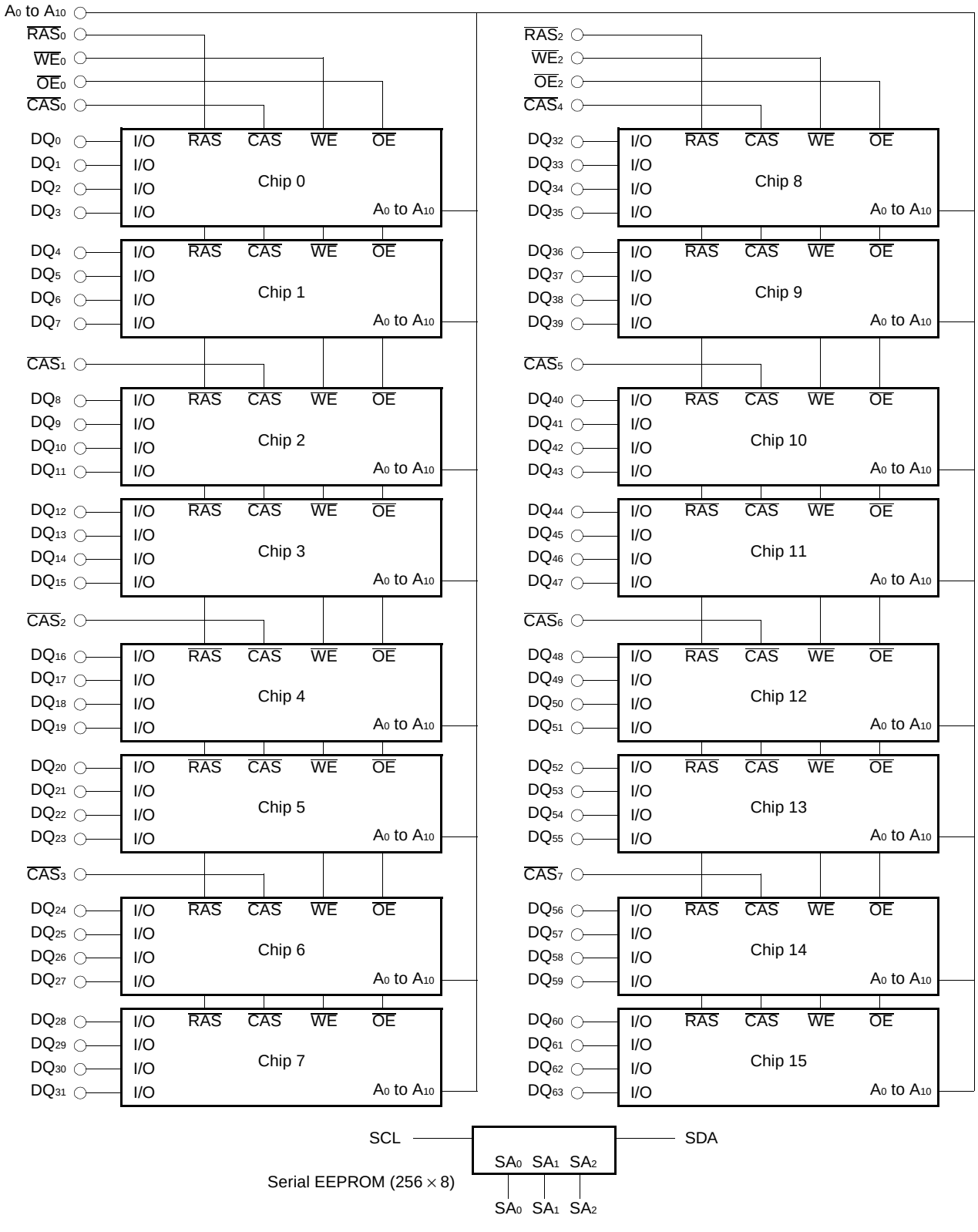
Fig.1 – BLOCK DIAGRAM



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■ SERIAL PRESENCE DETECT (SPD) TABLE

Byte	Function Described		Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
0	Number of Bytes Used by Module Manufacturer	14 Bytes	0	0	0	0	1	1	1	0
1	Total SPD Memory Size	256 Bytes	0	0	0	0	1	0	0	0
2	Memory Type	EDO	0	0	0	0	0	0	1	0
3	Number of Row Addresses	11 Addresses	0	0	0	0	1	0	1	1
4	Number of Column Addresses	11 Addresses	0	0	0	0	1	0	1	1
5	Number of Banks	1 Bank	0	0	0	0	0	0	0	1
6	Module Data Width (1)	64 Bits	0	1	0	0	0	0	0	0
7	Module Data Width (2)	+0 Bits	0	0	0	0	0	0	0	0
8	Module Interface Levels	LVTTL	0	0	0	0	0	0	0	1
9	$\overline{RAS}$ Access Time (t_{RAC})	60 ns	0	0	1	1	1	1	0	0
		70 ns	0	1	0	0	0	1	1	0
10	$\overline{CAS}$ Access Time (t_{CAC})	15 ns	0	0	0	0	1	1	1	1
		17 ns	0	0	0	1	0	0	0	1
11	Module Configuration Type (Parity or ECC or None)	None	0	0	0	0	0	0	0	0
12	Refresh Rate / Type	Normal	0	0	0	0	0	0	0	0
13	Primary DRAM Width	×4	0	0	0	0	0	1	0	0
14	Error Checking DRAM Data Width	None	0	0	0	0	0	0	0	0
15 to 31	Reserved for Future Offerings	—	—	—	—	—	—	—	—	—
32 to 63	Superset Information	—	—	—	—	—	—	—	—	—
64 to 127	Manufacturer's Information	—	—	—	—	—	—	—	—	—
128 to 255	Unused Storage Locations	—	—	—	—	—	—	—	—	—

Note: Any write operation must NOT be executed into the addresses of Byte 0 to Byte 127. Some or all data stored into Byte 0 to Byte 127 may be broken.

■ ABSOLUTE MAXIMUM RATINGS (See WARNING)

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	–0.5 to +4.6	V
Input Voltage	V_{IN}	–0.5 to +4.6	V
Output Voltage	V_{OUT}	–0.5 to +4.6	V
Short Circuit Output Current	I_{OUT}	–50 to +50	mA
Power Dissipation	P_D	16	W
Storage Temperature	T_{STG}	–55 to +125	°C

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

(Referenced to V_{SS})

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{CC}	3.0	3.0	3.6	V
Ground	V_{SS}	—	0	—	V
Input High Voltage, All Inputs	V_{IH}	2.0	—	V_{CC} + 0.3 V	V
Input Low Voltage, All Inputs*	V_{IL}	–0.3	—	0.8	V
Ambient Temperature	T_A	0	—	70	°C

Note: * Undershoots of up to –2.0 volts with a pulse width not exceeding 20 ns are acceptable.

WARNING: Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representative beforehand.

■ CAPACITANCE

(T_A = 25°C, f = 1 MHz, V_{CC} = +3.3 V)

Parameter		Symbol	Min.	Max.	Unit
Input Capacitance	A_0 to A_{10}	C_{IN1}	—	124	pF
	$\overline{RAS}_0$ and $\overline{RAS}_2$	C_{IN2}	—	60	pF
	$\overline{CAS}_0$ to $\overline{CAS}_7$	C_{IN3}	—	22	pF
	$\overline{WE}_0$ and $\overline{WE}_2$	C_{IN4}	—	61	pF
	$\overline{OE}_0$ and $\overline{OE}_2$	C_{IN5}	—	58	pF
	SCL	C_{IN6}	—	6	pF
	SA_0 to SA_2	C_{IN7}	—	7	pF
I/O Capacitance	DQ_0 to DQ_{63}	C_{DQ}	—	13	pF
	SDA	C_{SDA}	—	7	pF

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■ DC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted.)

Parameter	Notes		Symbol	Condition	Value		Unit
					Min.	Max.	
Output High Voltage	*1		V_{OH}	I_{OH} = –2 mA	2.4	—	V
Output Low Voltage	*1		V_{OL}	I_{OL} = 2 mA	—	0.4	V
Input Leakage Current		$\overline{RAS}$, $\overline{WE}$, $\overline{OE}$	$I_{I(L)}$	0 V ≤ V_{IN} ≤ V_{CC}, 3.0 V ≤ V_{CC} ≤ 3.6 V, V_{SS} = 0 V, all other pins not under test = 0 V	–37	37	µA
		$\overline{CAS}$			–17	17	
		Others			–80	80	µA
Output Leakage Current			$I_{O(L)}$	0 V ≤ V_{OUT} ≤ V_{CC}, 3.0 V ≤ V_{CC} ≤ 3.6 V Data out disabled	–10	10	µA
Operating Current (Average Power Supply Current)	*2	MB8504E064AB-60	I_{CC1}	$\overline{RAS}$ & $\overline{CAS}$ cycling, t_{RC} = min	—	1760	mA
		MB8504E064AB-70			—	1520	
Standby Current (Power Supply Current)	*2	TTL Level	I_{CC2}	$\overline{RAS}$ = $\overline{CAS}$ = V_{IH}	—	32	mA
		CMOS Level		$\overline{RAS}$ = $\overline{CAS}$ ≥ V_{CC} –0.2 V	—	16	
Refresh Current #1 (Average Power Supply Current)	*2	MB8504E064AB-60	I_{CC3}	$\overline{CAS}$ = V_{IH}, $\overline{RAS}$ = cycling, t_{RC} = min	—	1760	mA
		MB8504E064AB-70			—	1520	
Hyper Page Mode Current	*2	MB8504E064AB-60	I_{CC4}	$\overline{RAS}$ = V_{IL}, $\overline{CAS}$ = cycling, t_{HPC} = min	—	1440	mA
		MB8504E064AB-70			—	1280	
Refresh Current #2 (Average Power Supply Current)	*2	MB8504E064AB-60	I_{CC5}	$\overline{RAS}$ cycling, $\overline{CAS}$-before-$\overline{RAS}$, t_{RC} = min	—	1760	mA
		MB8504E064AB-70			—	1520	

Notes: *1. Referenced to V_{SS}.

*2. I_{CC} depends on the output load conditions and cycle rate. The specific values are obtained with the output open.
I_{CC} depends on the number of address change as $\overline{RAS}$ = V_{IL} and $\overline{CAS}$ = V_{IH} and V_{IL} > –0.3 V.
I_{CC1}, I_{CC3}, I_{CC4} and I_{CC5} are specified at one time of address change during $\overline{RAS}$ = V_{IL} and $\overline{CAS}$ = V_{IH}.
I_{CC2} is specified during $\overline{RAS}$ = V_{IH} and V_{IL} > –0.3 V.

■ AC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted.) Notes 1, 2, 3

No.	Parameter	Notes	Symbol	MB8504E064AB-60		MB8504E064AB-70		Unit
				Min.	Max.	Min.	Max.	
1	Time Between Refresh		t_{REF}	—	32.8	—	32.8	ms
2	Random Read/Write Cycle Time		t_{RC}	104	—	124	—	ns
3	Read-Modify-Write Cycle Time		t_{RWC}	138	—	162	—	ns
4	Access Time from $\overline{RAS}$	*4,7	t_{RAC}	—	60	—	70	ns
5	Access Time from $\overline{CAS}$	*5,7	t_{CAC}	—	15	—	17	ns
6	Column Address Access Time	*6,7	t_{AA}	—	30	—	35	ns
7	Output Hold Time		t_{OH}	3	—	3	—	ns
8	Output Hold Time from $\overline{CAS}$		t_{OHC}	5	—	5	—	ns
9	Output Buffer Turn On Delay Time		t_{ON}	0	—	0	—	ns
10	Output Buffer Turn Off Delay Time	*8	t_{OFF}	—	15	—	17	ns
11	Output Buffer Turn Off Delay Time from $\overline{RAS}$	*8	t_{OFR}	—	15	—	17	ns
12	Output Buffer Turn Off Delay Time from $\overline{WE}$	*8	t_{WEZ}	—	15	—	17	ns
13	Transition Time		t_T	1	50	1	50	ns
14	$\overline{RAS}$ Precharge Time		t_{RP}	40	—	50	—	ns
15	$\overline{RAS}$ Pulse Width		t_{RAS}	60	100000	70	100000	ns
16	$\overline{RAS}$ Hold Time		t_{RSH}	15	—	17	—	ns
17	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time		t_{CRP}	5	—	5	—	ns
18	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	*9,10	t_{RCD}	14	45	14	53	ns
19	$\overline{CAS}$ Pulse Width		t_{CAS}	10	—	13	—	ns
20	$\overline{CAS}$ Hold Time		t_{CSH}	40	—	50	—	ns
21	$\overline{CAS}$ Precharge Time (Normal)	*17	t_{CPN}	10	—	10	—	ns
22	Row Address Setup Time		t_{ASR}	0	—	0	—	ns
23	Row Address Hold Time		t_{RAH}	10	—	10	—	ns
24	Column Address Setup Time		t_{ASC}	0	—	0	—	ns
25	Column Address Hold Time		t_{CAH}	10	—	10	—	ns
26	Column Address Hold Time from $\overline{RAS}$		t_{AR}	24	—	24	—	ns
27	$\overline{RAS}$ to Column Address Delay Time	*11	t_{RAD}	12	30	12	35	ns
28	Column Address to $\overline{RAS}$ Lead Time		t_{RAL}	30	—	35	—	ns
29	Column Address to $\overline{CAS}$ Lead Time		t_{CAL}	23	—	28	—	ns
30	Read Command Setup Time		t_{RCS}	0	—	0	—	ns
31	Read Command Hold Time Referenced to $\overline{RAS}$	*12	t_{RRH}	0	—	0	—	ns

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(Continued)

No.	Parameter	Notes	Symbol	MB8504E064AB-60		MB8504E064AB-70		Unit
				Min.	Max.	Min.	Max.	
32	Read Command Hold Time Referenced to $\overline{CAS}$	*12	t_{RCH}	0	—	0	—	ns
33	Write Command Setup Time	*13,18	t_{WCS}	0	—	0	—	ns
34	Write Command Hold Time		t_{WCH}	10	—	10	—	ns
35	Write Command Hold Time from $\overline{RAS}$		t_{WCR}	24	—	24	—	ns
36	$\overline{WE}$ Pulse Width		t_{WP}	10	—	10	—	ns
37	Write Command to $\overline{RAS}$ Lead Time		t_{RWL}	15	—	17	—	ns
38	Write Command to $\overline{CAS}$ Lead Time		t_{CWL}	10	—	13	—	ns
39	DIN Setup Time		t_{DS}	0	—	0	—	ns
40	DIN Hold Time		t_{DH}	10	—	10	—	ns
41	Data Hold Time from $\overline{RAS}$		t_{DHR}	24	—	24	—	ns
42	$\overline{RAS}$ to $\overline{WE}$ Delay Time	*18	t_{RWD}	77	—	89	—	ns
43	$\overline{CAS}$ to $\overline{WE}$ Delay Time	*18	t_{CWD}	32	—	36	—	ns
44	Column Address to $\overline{WE}$ Delay Time	*18	t_{AWD}	47	—	54	—	ns
45	$\overline{RAS}$ Precharge Time to $\overline{CAS}$ Active Time (Refresh Cycles)		t_{RPC}	5	—	5	—	ns
46	$\overline{CAS}$ Setup Time (C-B-R Refresh)		t_{CSR}	0	—	0	—	ns
47	$\overline{CAS}$ Hold Time (C-B-R Refresh)		t_{CHR}	10	—	12	—	ns
48	Access Time from $\overline{OE}$	*7	t_{OEA}	—	15	—	17	ns
49	Output Buffer Turn Off Delay from $\overline{OE}$	*8	t_{OEZ}	—	15	—	17	ns
50	$\overline{OE}$ to $\overline{RAS}$ Lead Time for Valid Data		t_{OEL}	10	—	10	—	ns
51	$\overline{OE}$ to $\overline{CAS}$ Lead Time		t_{COL}	5	—	5	—	ns
52	$\overline{OE}$ Hold Time Referenced to $\overline{WE}$	*14	t_{OEH}	5	—	5	—	ns
53	$\overline{OE}$ to Data in Delay Time		t_{OED}	15	—	17	—	ns
54	$\overline{RAS}$ to Data in Delay Time		t_{RDD}	15	—	17	—	ns
55	$\overline{CAS}$ to Data in Delay Time		t_{CDD}	15	—	17	—	ns
56	DIN to $\overline{CAS}$ Delay Time	*15	t_{DZC}	0	—	0	—	ns
57	DIN to $\overline{OE}$ Delay Time	*15	t_{DZO}	0	—	0	—	ns
58	$\overline{OE}$ Precharge Time		t_{OEP}	8	—	8	—	ns
59	$\overline{OE}$ Hold Time Referenced to $\overline{CAS}$		t_{OECH}	10	—	10	—	ns
60	$\overline{WE}$ Precharge Time		t_{WPZ}	8	—	8	—	ns
61	$\overline{WE}$ to Data in Delay Time		t_{WED}	15	—	17	—	ns
62	Hyper Page Mode $\overline{RAS}$ Pulse Width		t_{RASP}	—	100000	—	100000	ns

(Continued)

(Continued)

No.	Parameter	Notes	Symbol	MB8504E064AB-60		MB8504E064AB-70		Unit
				Min.	Max.	Min.	Max.	
63	Hyper Page Mode Read/Write Cycle Time		t_{HPC}	25	—	30	—	ns
64	Hyper Page Mode Read-Modify-Write Cycle Time		t_{HPRWC}	69	—	79	—	ns
65	Access Time from $\overline{CAS}$ Precharge	*7,16	t_{CPA}	—	35	–	40	ns
66	Hyper Page Mode $\overline{CAS}$ Precharge Time		t_{CP}	10	—	10	—	ns
67	Hyper Page Mode $\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge		t_{RHCP}	35	—	40	—	ns
68	Hyper Page Mode $\overline{CAS}$ Precharge to $\overline{WE}$ Delay Time	*18	t_{CPWD}	52	—	59	—	ns

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Notes: *1. An initial pause ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH}) of 200 µs is required after power-up followed by any eight $\overline{RAS}$-only cycles or eight $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles ($\overline{WE}$ = V_{IH}) before proper device operation is achieved. If an internal refresh counter is used, a minimum of eight $\overline{CAS}$-before-$\overline{RAS}$ initialization cycles are required instead of eight $\overline{RAS}$ cycles.

*2. AC characteristics assume t_T = 2 ns.

*3. V_{IH} (min) and V_{IL} (max) are reference levels for measuring the timing of input signals. Transition times are measured between V_{IH} (min) and V_{IL} (max).

*4. Assumes that $t_{RCD} \leq t_{RCD}$ (max), $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} and/or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} will be increased by the amount that t_{RCD} and/or t_{RAD} exceeds the value shown.

*5. If $t_{RCD} \geq t_{RCD}$ (max), $t_{RAD} \geq t_{RAD}$ (max), and $t_{ASC} \geq t_{AA} - t_{CAC} - t_T$, access time is t_{CAC}.

*6. If $t_{RAD} \geq t_{RAD}$ (max) and $t_{ASC} \leq t_{AA} - t_{CAC} - t_T$, access time is t_{AA}.

*7. Measured with a load equivalent to two TTL loads and 100 pF.

*8. t_{OFF}, t_{OEZ}, t_{OFR} and t_{WEZ} are specified that output buffer change to high-impedance state.

*9. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, access time is controlled exclusively by t_{CAC} or t_{AA}.

*10. t_{RCD} (min) = t_{RAH} (min) + 2t_T + t_{ASC} (min).

*11. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max) limit, access time is controlled exclusively by t_{CAC} or t_{AA}.

*12. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

*13. t_{WCS} is specified as a reference point only. If $t_{WCS} \geq t_{WCS}$ (min) the data output pin will remain High-Z state through entire cycle.

*14. Assumes that $t_{WCS} < t_{WCS}$ (min).

*15. Either t_{DZC} or t_{DZO} must be satisfied.

*16. t_{CPA} is access time from the selection of a new column address (caused by changing $\overline{CAS}$ from “L” to “H”). Therefore, if t_{CP} becomes long, t_{CPA} also becomes longer than t_{CPA} (max).

*17. Assumes $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle.

*18. t_{WCS}, t_{CWD}, t_{RWD}, t_{AWD}, and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as an electrical characteristic only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and D_{OUT} pin will maintain high-impedance state thoughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), $t_{AWD} \geq t_{AWD}$ (min), and $t_{CPWD} \geq t_{CPWD}$ (min), the cycle is a read-modify-write cycle and data from the selected cell will appear at the D_{OUT} pin. If neither of the above conditions is satisfied, the cycle is a delayed write cycle and invalid data will appear the D_{OUT} pin, and write operation can be executed by satisfying t_{RWL}, t_{CWL}, t_{RAL} and t_{CAL} specifications.

*Source: See MB81V17405A Data Sheet for details on the electricals.

■ SERIAL PRESENCE DETECT (SPD) FUNCTION

1. PIN DESCRIPTIONS

SCL (Serial Clock)

SCL input is used to clock all data input/output of SPD.

SDA (Serial Data)

SDA is a common pin used for all data input/output of SPD. The SDA pull-up resistor is required due to the open-drain output.

SA_0, SA_1, SA_2 (Address)

Address inputs are used to set the least significant three bits of the eight bits slave address. The address inputs must be fixed to select a particular module and the fixed address of each module must be different each other.

2. SPD OPERATIONS

CLOCK and DATA CONVENTION

Data states on the SDA can change only during SCL=Low. SDA state changes during SCL=High are indicated start and stop conditions. Refer to Fig.2 below.

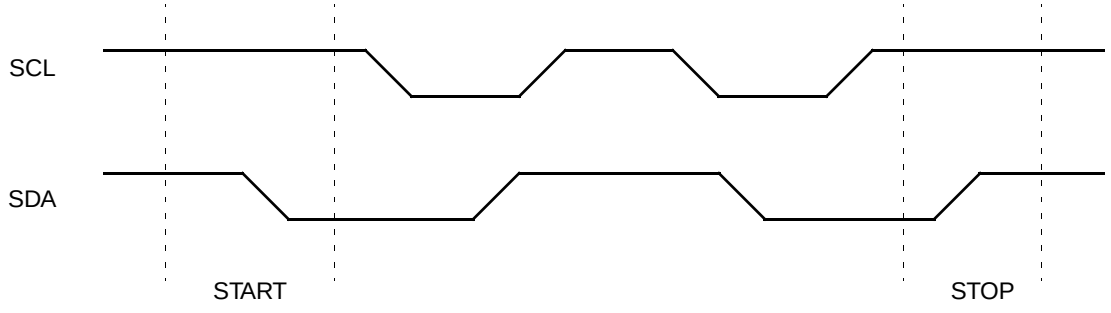
START CONDITION

All commands are preceded by a start condition, which is a transition of SDA state from High to Low when SCL=High. SPD will not respond to any command until this condition has been met.

STOP CONDITION

All read or write operation must be terminated by a stop condition, which is a transition of SDA state from Low to High when SCL=High. The stop condition is also used to make the SPD into the state of standby power mode after a read sequence.

Fig.2 – START AND STOP CONDITIONS



START = High to Low transition of SDA state when SCL is High
STOP = Low to High transition of SDA state when SCL is High

ACKNOWLEDGE

Acknowledge is a software convention used to indicate successful data transfer. The transmitting device, either master or slave, will release the bus after transmitting eight bits. During the ninth clock cycle the receiver will put the SDA line to Low in order to acknowledge that it received the eight bits of data.

The SPD will respond with an acknowledge when it received the start condition followed by slave address issued by master.

In the read operation, the SPD will transmit eight bits of data, release the SDA line and monitor the line for an acknowledge. If an acknowledge is detected and no stop condition is issued by master, the SPD will continue to transmit data. If an acknowledge is not detected, the SPD will terminated further data transmissions. The master must then issue a stop condition to return the SPD to the standby power mode.

In the write operation, upon receipt of eight bits of data the SPD will respond with an acknowledge, and await the next eight bits of data, again responding with an acknowledge until the stop condition is issued by master.

SLAVE ADDRESS ADDRESSING

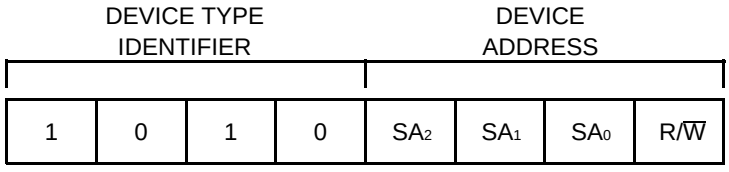
Following a start condition, the master must output the eight bits slave address. The most significant four bits of the slave address are device type identifier. For the SPD this is fixed as 1010[B]. Refer to the Fig.3 below.

The next three significant bits are used to select a particular device. A system could have up to eight SPD devices –namely up to eight modules– on the bus. The eight addresses for eight SPD devices are defined by the state of the SA_0, SA_1 and SA_2 inputs.

The last bit of the slave address defines the operation to be performed. When R/$\overline{W}$ bit is “1”, a read operation is selected, when R/$\overline{W}$ bit is “0”, a write operation is selected.

Following the start condition, the SPD monitors the SDA line comparing the slave address being transmitted with its slave address (device type and state of SA_0, SA_1, and SA_2 inputs). Upon a correct compare the SPD outputs an acknowledge on the SDA line. Depending on the state of the R/$\overline{W}$ bit, the SPD will execute a read or write operation.

Fig.3 – SLAVE ADDRESS

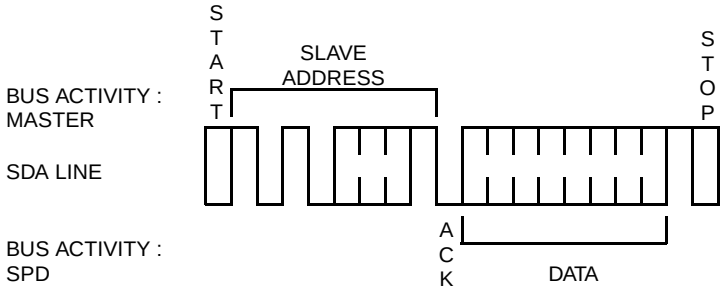


3. READ OPERATIONS

CURRENT ADDRESS READ

Internally the SPD contains an address counter that maintains the address of the last data accessed, incremented by one. Therefore, if the last access (either a read or write operation) was to address(n), the next read operation would access data from address(n+1). Upon receipt of the slave address with the R/$\overline{W}$ bit = "1", the SPD issues an acknowledge and transmits the eight bits of data during the next eight clock cycles. The master terminates this transmission by issuing a stop condition, omitting the ninth clock cycle acknowledge. Refer to Fig.4 for the sequence of address, acknowledge and data transfer.

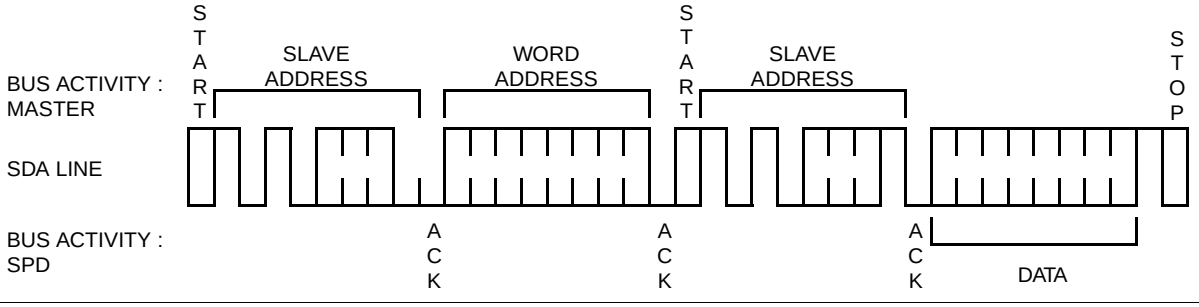
Fig.4 – CURRENT ADDRESS READ



RANDOM READ

Random Read operations allow the master to access any memory location in a random manner. Prior to issuing the slave address with the R/$\overline{W}$ bit = "1", the master must first perform a "dummy" write operation on the SPD. The master issues the start condition, and the slave address followed by the word address. After the word address acknowledge, the master immediately reissues the start condition and the slave address with the R/$\overline{W}$ bit = "1". This will be followed by an acknowledge from the SPD and then by the eight bits of data. The master terminates this transmission by issuing a stop condition, omitting the ninth clock cycle acknowledge. Refer to Fig.5 for the sequence of address, acknowledge and data transfer.

Fig.5 – RANDOM READ

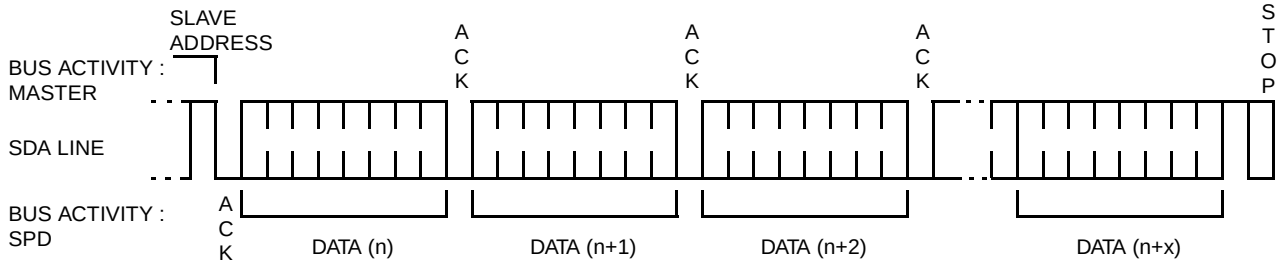


SEQUENTIAL READ

Sequential Read can be initiated as either a current address read or random read. The first data are transmitted as with the other read mode, however, the master now responds with an acknowledge, indicating it requires additional data. The SPD continues to output data for each acknowledge received. The master terminates this transmission by issuing a stop condition, omitting the ninth clock cycle acknowledge. Refer to Fig.6 for the sequence of address, acknowledge and data transfer.

The data output is sequential, with the data from address(n) followed by the data from address(n+1). The address counter for read operations increments all address bits, allowing the entire memory contents to be serially read during one operation. At the end of the address space (address 255), the counter “rolls over” to address 0 and the SPD continues to output data for each acknowledge received.

Fig.6 – SEQUENTIAL READ



4. DC CHARACTERISTICS

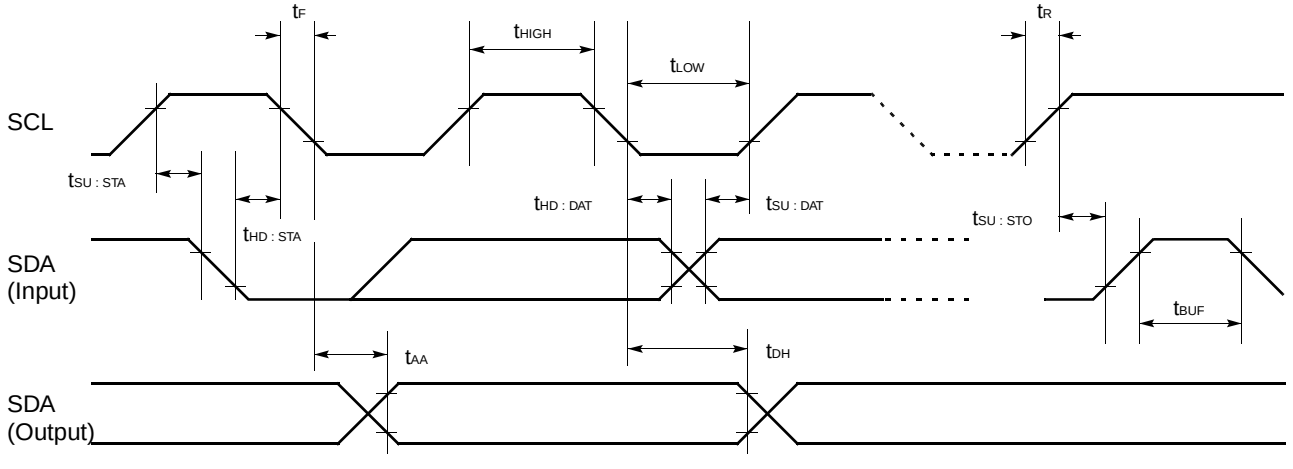
Parameter	Note	Test Condition	Symbol	Min.	Max.	Unit
Input Leakage Current		$0 V \le V_{IN} \le V_{CC}$	S_{ILI}	–10	10	µA
Output Leakage Current		$0 V \le V_{OUT} \le V_{CC}$	S_{ILO}	–10	10	µA
Output Low Voltage	*1	I_{OL} = 3.0 mA	S_{VOL}	—	0.4	V

Note: *1 Referenced to V_{SS}.

5. AC CHARACTERISTICS

No.	Parameter	Symbol	Min.	Max.	Unit
1	SCL Clock Frequency	f_{SCL}	0	100	kHz
2	Noise Suppression Time Constant at SCL, SDA Inputs	T_I	—	100	ns
3	SCL Low to SDA Data Out Valid	t_{AA}	0.3	3.5	µs
4	Time the Bus Must Be Free before a New Transmission Can Start	t_{BUF}	4.7	—	µs
5	Start Condition Hold Time	$t_{HD:STA}$	4.0	—	µs
6	Clock Low Period	t_{LOW}	4.7	—	µs
7	Clock High Period	t_{HIGH}	4.0	—	µs
8	Start Condition Setup Time	$t_{SU:STA}$	4.7	—	µs
9	Data In Hold Time	$t_{HD:DAT}$	0	—	µs
10	Data In Setup Time	$t_{SU:DAT}$	250	—	ns
11	SDA and SCL Rise Time	t_R	—	1	µs
12	SDA and SCL Fall Time	t_F	—	300	ns
13	Stop Condition Setup Time	$t_{SU:STO}$	4.7	—	µs
14	Data Out Hold Time	t_{DH}	100	—	ns
15	Write Cycle Time	t_{WR}	—	15	ms

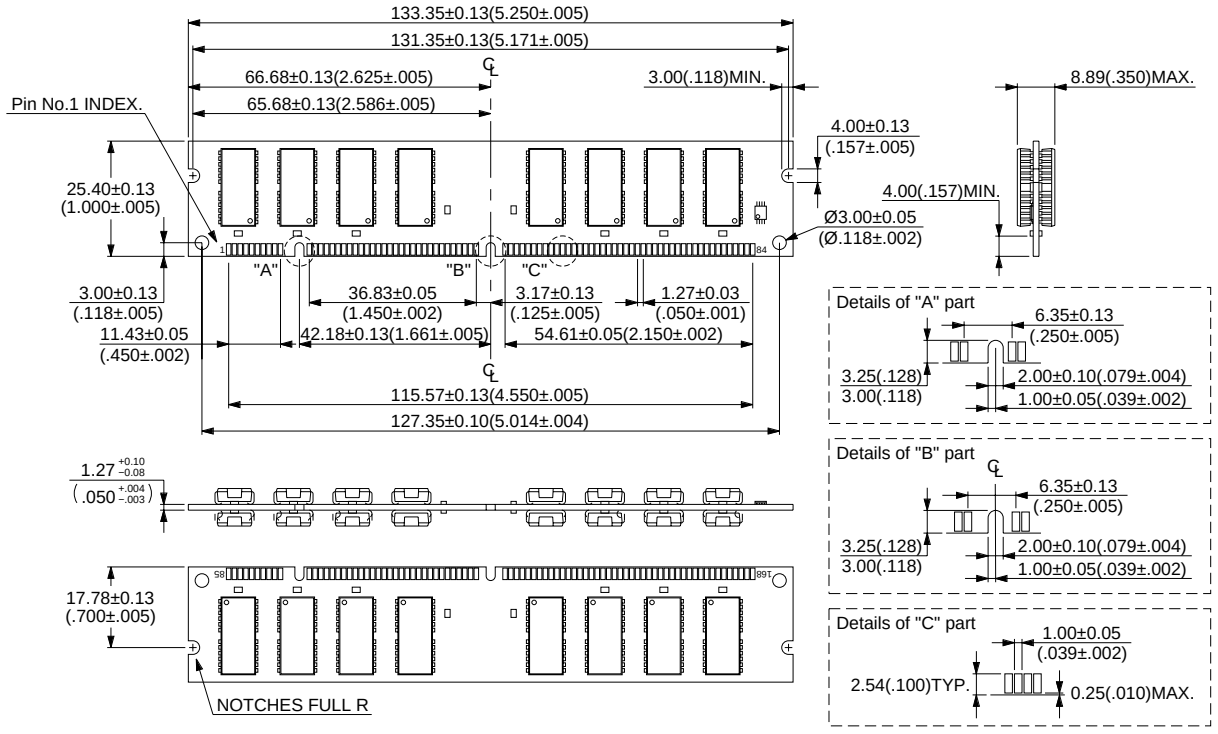
Fig.7 – TIMING WAVEFORM



MB8504E064AB-60/-70

■ PACKAGE DIMENSION

168-pin plastic DIMM
(MDS-168P-P11)



Dimensions in mm (inches)

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